

METHOD OF FORMING A CONDUCTIVE PATTERN OF A SEMICONDUCTOR DEVICE AND  
METHOD OF MANUFACTURING A NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE USING  
THE SAME

Application No. NEW - Attorney Docket No. SEC.1143

Inventor(s): Don-Woo LEE et al.

FIG. 1A  
(PRIOR ART)

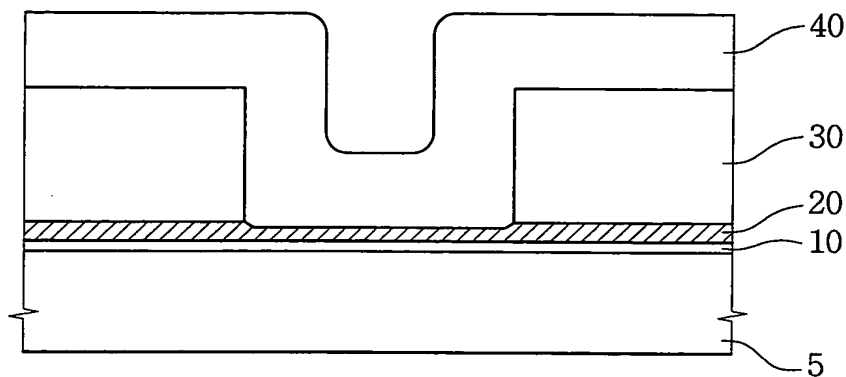
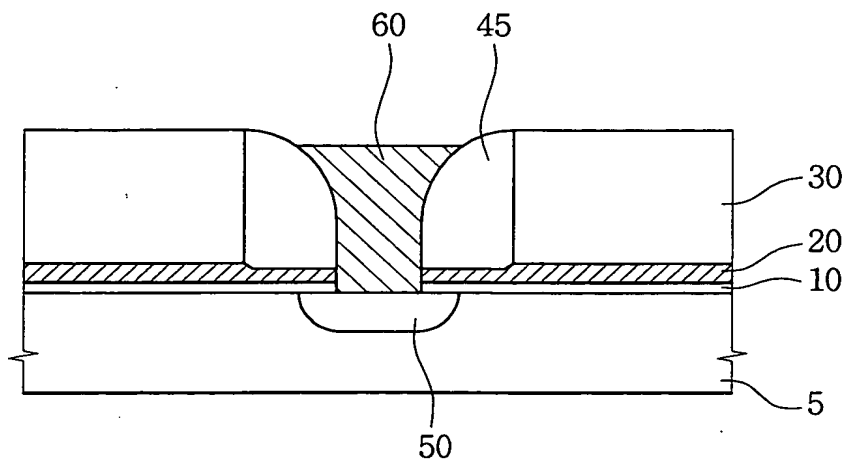


FIG. 1B  
(PRIOR ART)



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FIG. 1C  
(PRIOR ART)

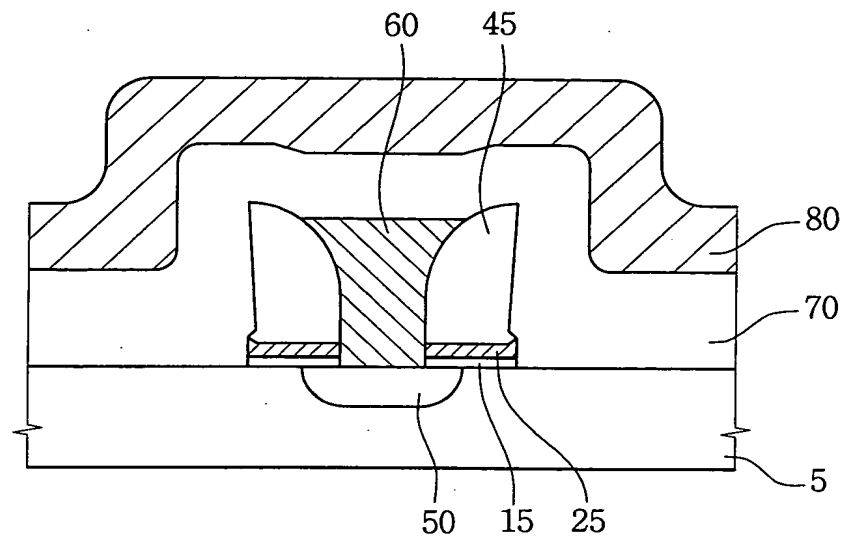
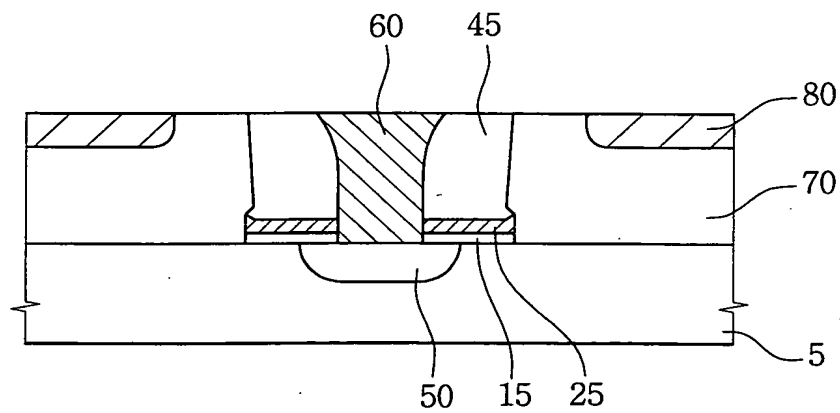


FIG. 1D  
(PRIOR ART)



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FIG. 1E  
(PRIOR ART)

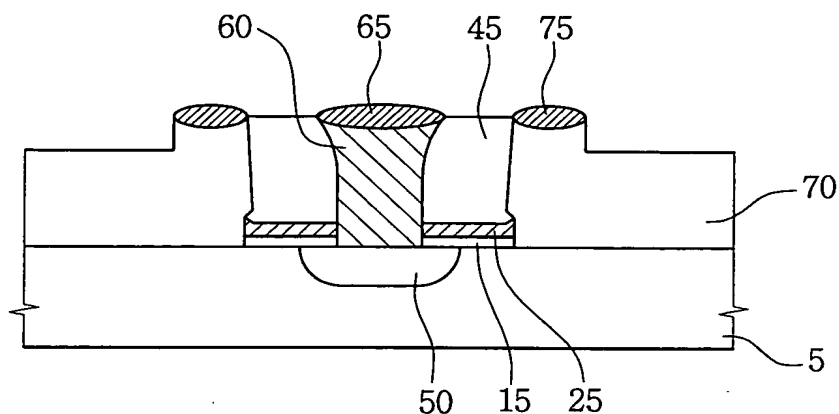
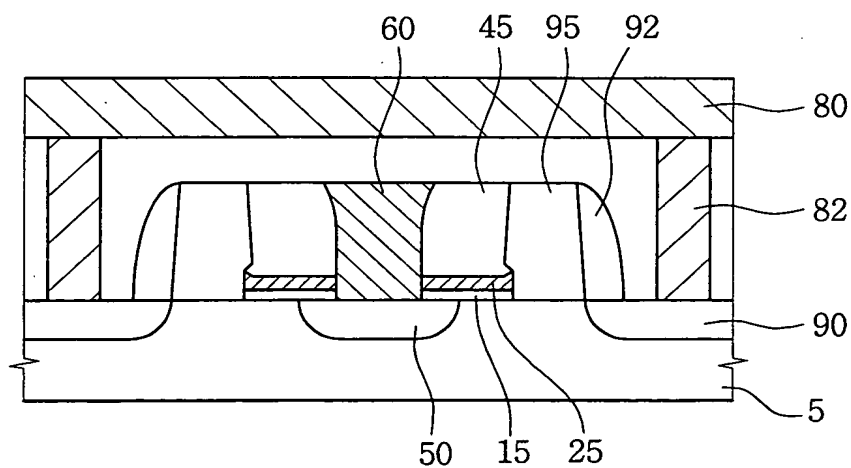


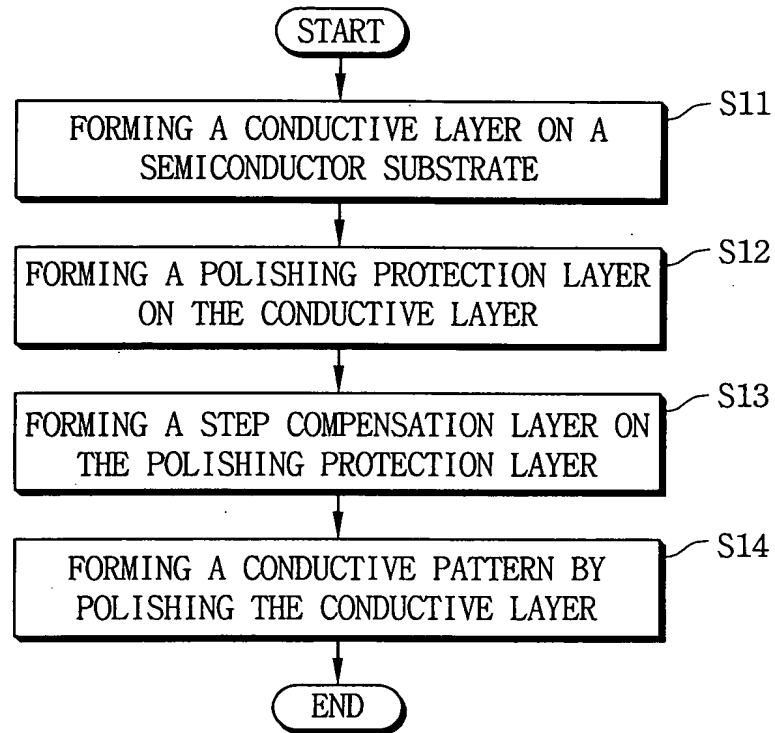
FIG. 1F  
(PRIOR ART)



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FIG.2



METHOD OF FORMING A CONDUCTIVE PATTERN OF A SEMICONDUCTOR DEVICE AND  
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FIG. 3A

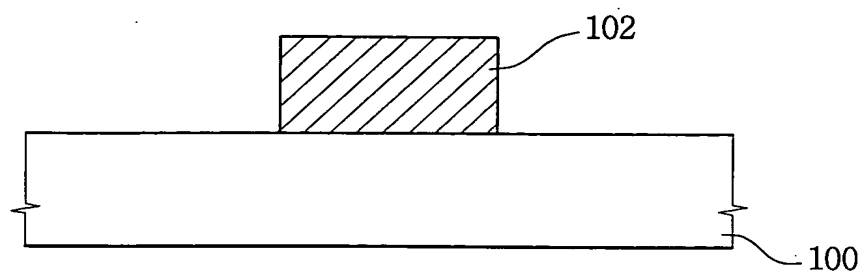
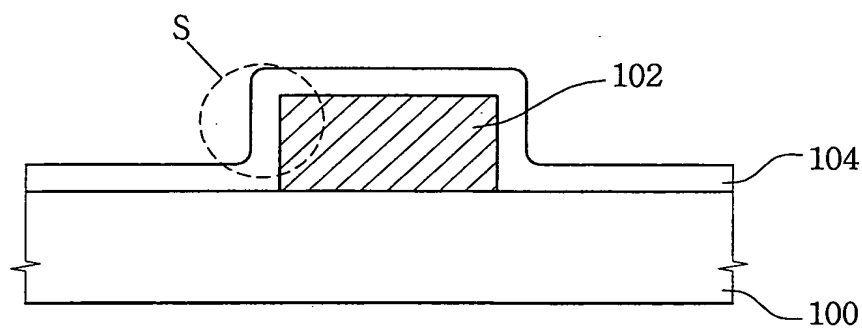


FIG. 3B



METHOD OF FORMING A CONDUCTIVE PATTERN OF A SEMICONDUCTOR DEVICE AND  
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FIG. 3C

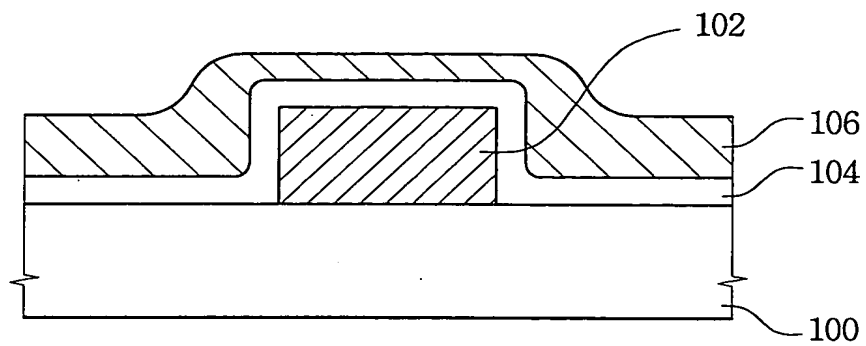
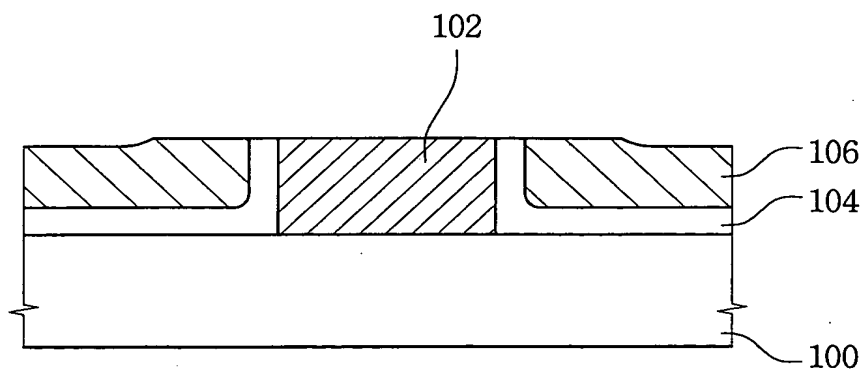


FIG. 3D

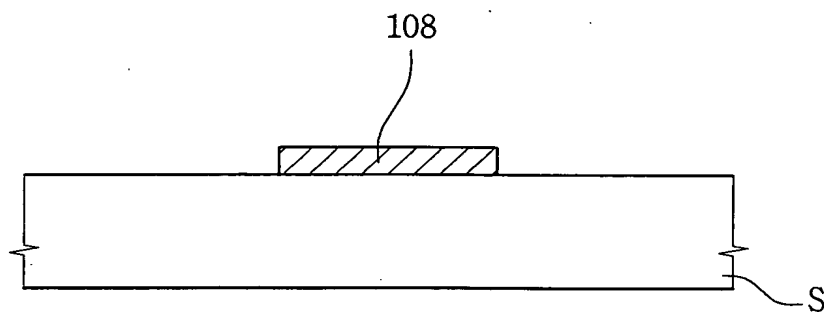


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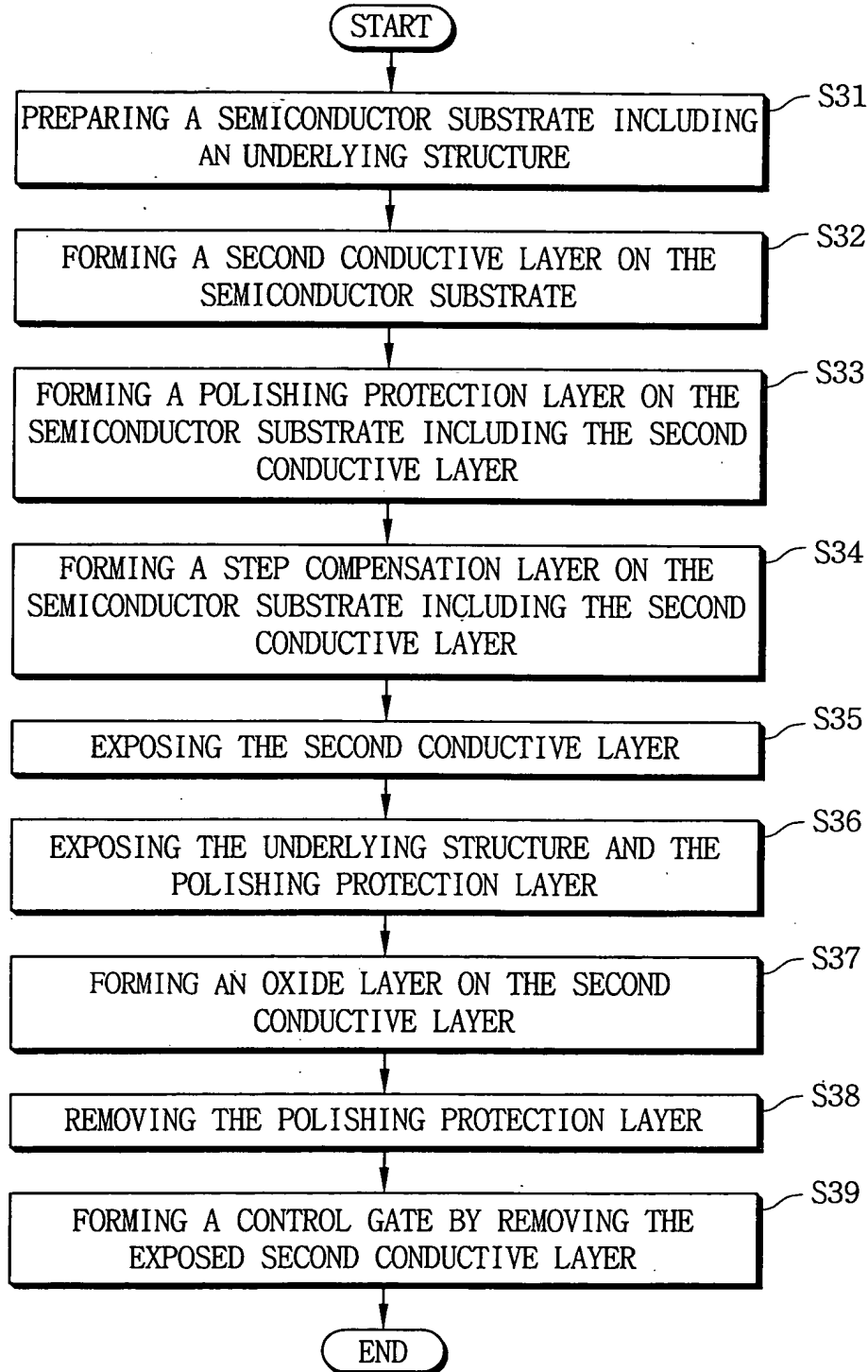
FIG. 3E



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FIG. 4





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FIG. 5A

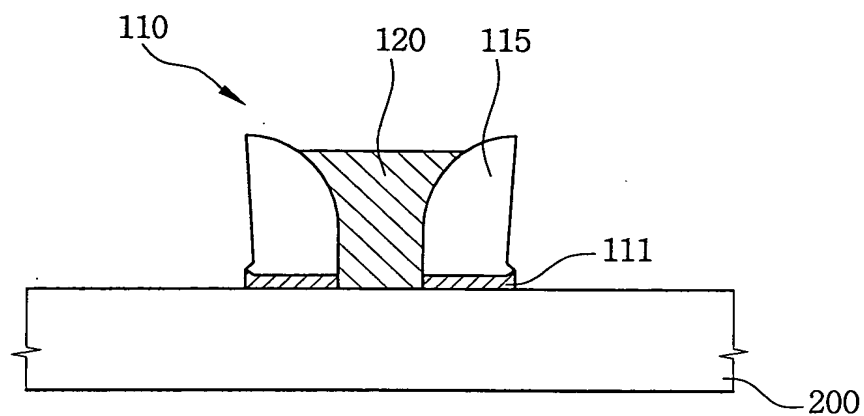
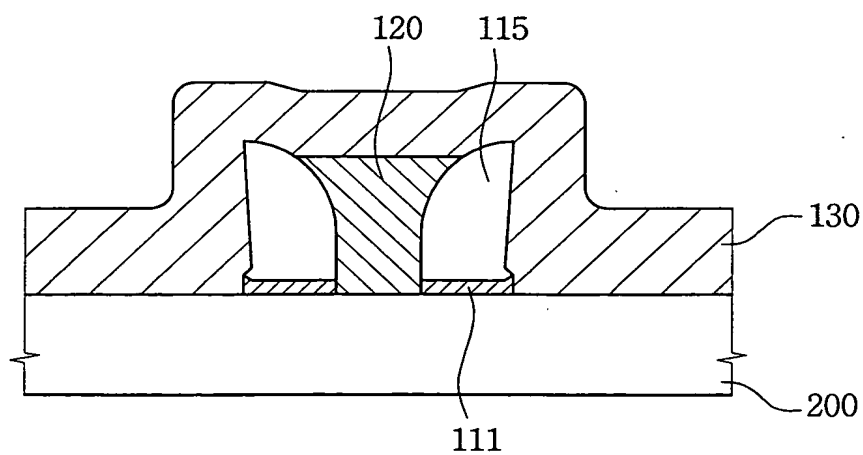


FIG. 5B



METHOD OF FORMING A CONDUCTIVE PATTERN OF A SEMICONDUCTOR DEVICE AND  
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FIG. 5C

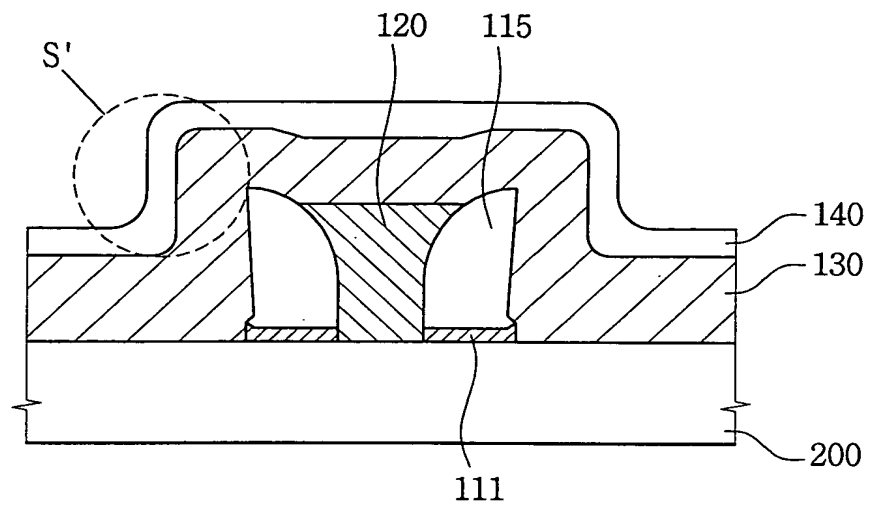
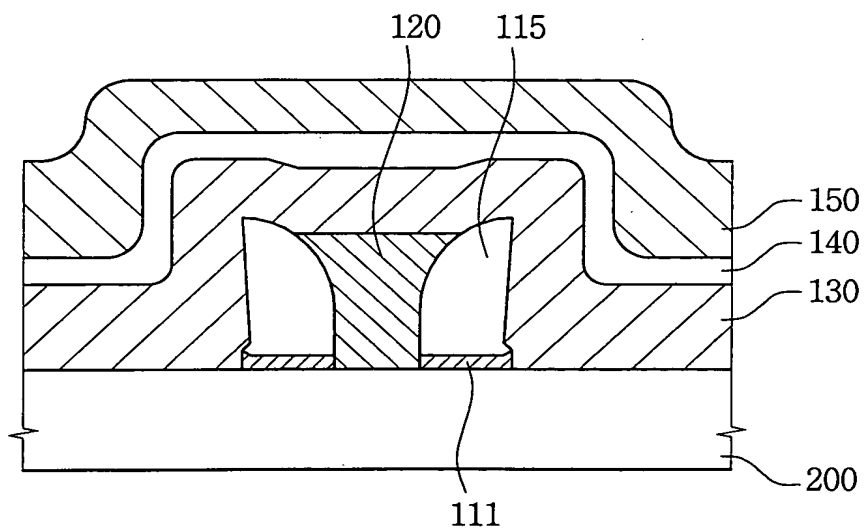


FIG. 5D



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FIG. 5E

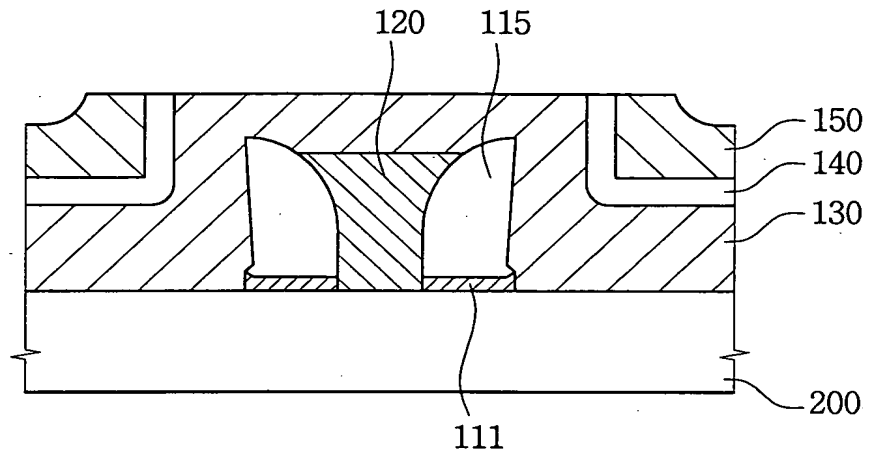
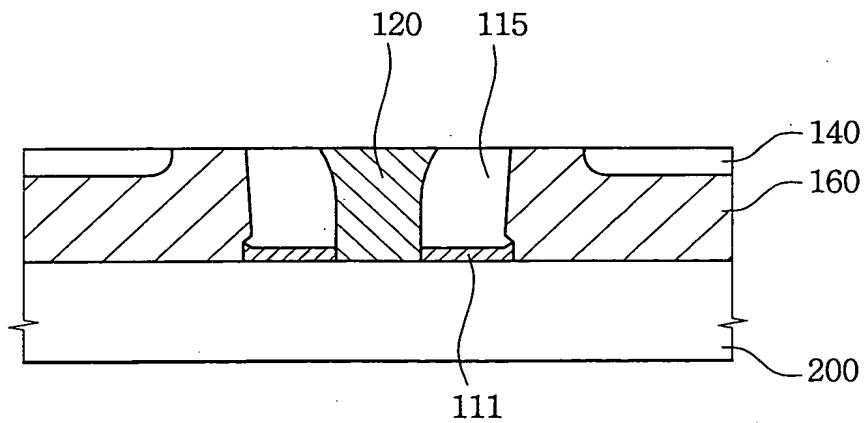


FIG. 5F



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FIG. 5G

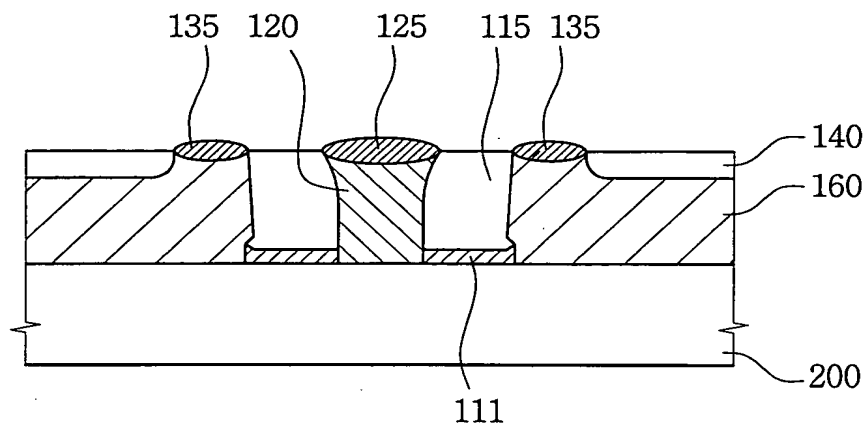
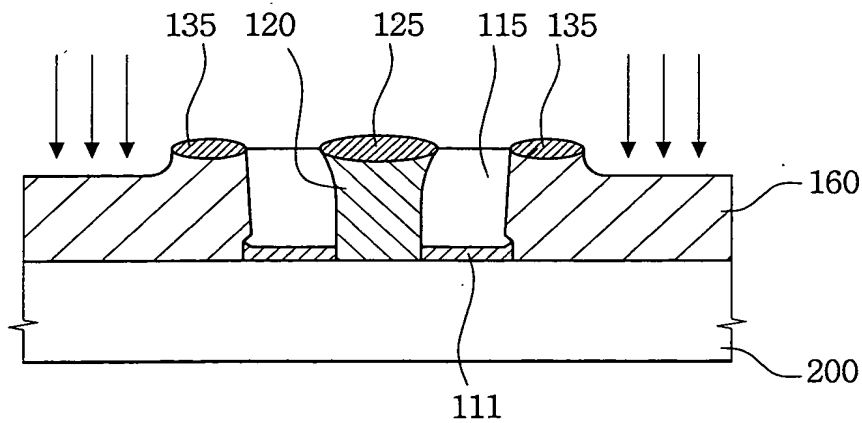


FIG. 5H



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A cross-sectional view of a semiconductor device. A substrate 200 is shown at the bottom. On top of the substrate, there are three pillars. The pillars are labeled 135, 120, 125, 115, and 135 from left to right. The pillars are connected by a layer 111. The top surface of the substrate is labeled 132.